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LEE, HONG, DEGERMAN, KANG & SCHMADEKA, P.C.
801 SOUTH FIQUEROA STREET
14TH FLOOR
LOS ANGELES, CA 90017

EXAMINER	
MATTHEW, AARON D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,847	OK, JAE CHUL	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/058847.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

1. The drawings are objected to because Fig. 1 is mislabeled, "Backbround Art." This should be changed to read, "Background Art". Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following references mentioned in the description: the break point address and the break enable signal outputted to the memory break controller, (on page 8, line 17). Corrected drawing sheets are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

1. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:
    - "...observing a change state and flow of an address and a data of the specific data memory in a data memory." Page 3, lines 22-23;
    - "...host computer 10 is being operation..." page 8, lines 9-10;
    - "According to judgement result, in case that the processor core 40 writes a data..." page 9, lines 19-20;

- "The data of a specific address of the data memory (70) read by the processor core 40 has an arithmetic and logical operation relation with a data value of a difference address or a correlation with a specific address of the data memory 70." Page 10, lines 4-7;
- "In case of executing continuously, the memory break controller 50 reads A2, so that addresses of every memory related until the next A2 value is written and their contents are outputted." Page 12, lines 17-19;
- "...an error that an erroneous calculation is inputted a during processing or a data memory is erroneously assigned is quickly sensed." Page 14, lines 7-8;
- "...a program development environment is set similar to an environment that the processor is substantially operated. Thus, a time and an expense for developing a program can be also saved." Page 14, lines 11-13.

2. The disclosure is objected to because of the following:

The example program beginning at the bottom of page 11 is unclear and appears illogical in places. It is suggested by the examiner that this section of the specification be rewritten, so as to clarify the example to help it serve its purpose in clarifying the disclosure of applicant's invention. Some sources of confusion in the example are as follows:

- The equation, A2 = A2 + (A1*A2), appears to be illogical, and if it has been entered correctly into the specification, requires more explanation.
- Language such as, "the memory break controller 50 reads A2, so that addresses of every memory related until the next A2 value is written and

their contents are outputted," on page 12, lines 17-19, is difficult to interpret, and should be revised.

- A2 is, at times, treated as a value, "(s)ince A2 is identical to the address to be observed," (page 13, line 2), and, at times, is treated as a system component capable of performing system functions, "...after A2 is sensed, it is determined whether it is reading or writing," (page 13, lines 7-8).

Appropriate correction is required.

Claim Objections

3. Claims 1-17 have been examined.
4. Claims 1-17 objected to because of the following informalities:
   - "Data", is a plural noun, and should not be referred to as, "a data." This error is found in the following places in the claim language:
     i. claim 1, line 3
     ii. claim 3, line 2
     iii. claim 8, line 6
     iv. claim 11, lines 6 and 7
     v. claim 12, lines 5-7
     vi. claim 13, line 1
     vii. claim 14, line 1

viii. claim 15, line 4

ix. claim 16, lines 11-13

x. claim 17, line 1

The examiner suggests changing the above mentioned references to "a data" to read, "the data" or just "data" as is deemed appropriate in the context of the claim language.

- the phrase, "...every memory which are read from or written..." in claim 7, lines 2-3, is unclear. The examiner suggests changing the phrase to read, "...every memory which is read from or written to..."
- the word, "address", on line 1, claim 12, should be changed to, "addresses"
- line 2 of claim 4 should be changed to read, "...data flow and change of the address..."
- line 12 of claim 9 should be changed to read, "...suspend the processor core,"

Appropriate correction is required.

5. Claims 2, 5, 6 and 10 are objected to based on their dependence on the above-mentioned claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 11-14 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 7, the claim language recites the following limitation: "...it outputs addresses and data of every memory which are read from or written in the processor core..." The specification specifically states that the debugging apparatus of the present invention is to include a single data memory, (see page 6, lines 1-10). The language, "every memory", in the above-mentioned limitation, suggests multiple memories available to the processor core, which is not taught in the specification. The examiner suggests changing the limitation to read, "...it outputs every address

and data which is read from or written to the data memory by the processor core..." to be more in line with the teachings of the specification.

Claim 11 describes a method in which two addresses are compared, are found to be identical, some flags are possibly enabled, and the addresses are compared again. If the addresses are then found to not be identical, an additional step is disclosed. The examiner can find no reasonable explanation in the claim language, or in the specification, as to why the addresses would possibly not be identical in the second comparison step. The specification, therefore, is not considered enabling for the limitation described in claim 11, in which an address and data of the data memory are transmitted in the event of a non-identical result of the second comparison step.

Regarding claims 13 and 17, the phrase, "next data memory," on line 2 suggests multiple memories available to the processor core, which is not taught in the specification. The specification specifically states that the debugging apparatus of the present invention is to include a single data memory, (see page 6, lines 1-10). The examiner suggests changing the limitation to read, "a next address of the data memory to be used...", and believes this alteration is in line with the intended scope of the claim.

Claims 12-14 are rejected based on their dependence on claim 11.

7. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the phrase, "when the address is sensed to be identical," on lines 10-11, is confusing. It is unclear what the address is sensed to be identical to. If the phrase is meant to teach that the address is sensed to be identical to the break point address, the examiner considers the phrase to be redundant. The limitation of, "recognizing an address as a break point address," presupposes that said address is identical to the break point address. The examiner suggests removing the above-mentioned phrase from the claim language.

Claim 5 recites the limitation "the control signal inputted from the debugger controller" in line 4. There is insufficient antecedent basis for this limitation in the claim. The examiner suggests changing the limitation to read, "...a control signal..."

Claims 5 and 8 recite the limitation "the data of the break point address" in lines 10 and 14, respectively. There is insufficient antecedent basis for this limitation in the claims. Prior to this limitation in claims 5 and 8, there is no mention of data being sent that is associated with the break point address. Sending a break point address value does not inherently comprise sending data that corresponds to the break point address value. The examiner suggests either adding a limitation in the claim

language prior to the aforementioned limitation, that describes data being sent along with the break point address value, or changing the aforementioned limitation to read, "storing data that corresponds to the break point address..." Appropriate correction is required.

Regarding claim 7, the limitation, "when the address trace check flag is enabled, it outputs addresses and data of every memory..." on lines 1-2, it is indefinite as to what the word "it" refers. The language appears to teach that the address trace check flag is outputting addresses and data, but the flag has not been disclosed with this capability. The examiner suggests replacing the word, "it", with an appropriate identifier for the component of the apparatus that is responsible for outputting addresses and data in the claim.

Regarding claim 9, the phrase, "outputting an address of a data memory to be observed, that is a break point address and a break enable signal," on lines 2-3, is unclear. It is indefinite as to what "that is" refers. The examiner suggests changing the language of the claim to read, "outputting a break enable signal and a break point address of a data memory to be observed, when a processor is switched to a debugging mode." This change should not change to scope of the claim language in any way, and is meant only to improve clarity. Appropriate correction is required.

Claim 9 recites the limitation "processor core" in line 10. There is insufficient antecedent basis for this limitation in the claim. It is unclear if the "processor" on lines 3, 5 and 16 is referring to the same or different entities as the "processor core" on lines 10, 12, 13, and 15. If they refer to the same entity, the language should be changed so as to be consistent throughout the claim. The language of the dependent claims should also be changed accordingly to maintain consistency, as it appears that the words "processor" and "processor core" are interchanged throughout the dependent claims. Appropriate correction is required.

Claim 11 recites the limitations "the address trace check flag", "the data check flag" and "the memory break control register" in lines 7 and 8. There is insufficient antecedent basis for these limitations in the claim. The limitations would appear to have sufficient antecedent basis if claim 11 was dependent on claim 10, instead of claim 9.

Claim 12 recites the limitation "the step of comparing address" in line 1. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to which step of comparing addresses in claim 11 this refers.

Regarding claims 13 and 17, the claims recite the limitation, "in case of reading a data upon judgement," on lines 1-2, which creates confusion as to when the event of reading data is taking place. The phrase could be read to mean that data is to be

read once judgement has been made, or to mean, in case it is judged that data was being read. The examiner assumes that the latter is appropriate, and suggests changing the claim language to read, "...wherein, if the processor core reads the data, an address..." Appropriate correction is required.

Regarding claim 14, the claim recites the limitation, "in case of writing a data in the judging step," on lines 1-2, which creates confusion as to when the event of writing data is taking place. The phrase could be read to mean that data is being written once judgement has been made, or to mean, in case it is judged that data was being written. The examiner assumes that the latter is appropriate, and suggests changing the claim language to read, "...wherein, if the processor core writes the data, an address..." Appropriate correction is required.

Regarding claim 16, the limitation, "a step in which when a processor is switched into a debugging mode, an address of a data memory to be observed, that is, a break point address, and a break enable signal are outputted," on lines 3-5, is unclear. It is indefinite as to what is being outputted. The examiner suggests changing the language to read, "a step in which when a processor is switched into a debugging mode, a break point address of a data memory to be observed and a break enable signal are outputted." This change should not change to scope of the claim language in any way, and is meant only to improve clarity. Appropriate correction is required.

Claims 2-4, 6, 10 and 15 are rejected based on the rejections of claims 1, 3, 5, 9 and 11 above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 5, 6, 8-12 and 14are rejected under 35 U.S.C. 102(e) as being anticipated by Waldie et al, (U.S. Patent Application Publication 2002/0065646 A1).

Regarding claim 1, Waldie teaches a debugging apparatus comprising:

- A processor core operated by a program stored in a program memory to read data stored in a data memory or write data, (note par. 0032);
- A debugger controller for performing a debugging on the processor core, (see par. 0029, lines 20-23), upon receipt of a command from a host computer, (note par. 0030, lines 1-4), and outputting a data break point address, (note par. 0075, lines 1-4); and

- A memory break controller for observing an address of a data memory used by the processor core, recognizing and address as a break point address to output a break signal to the debugger controller and the processor core to suspend the operation of the processor core, (see par. 0052 and 0050), and transmitting a corresponding address and data to the host computer through the debugger controller, (note, again, that the debug system is controlled by the debug controller, and see par. 0075, lines 26-34, in which the host may receive the information in the storage registers in the event of a breakpoint being detected).

Regarding claim 2, see, again, par. 0032, in which the processor core is coupled to a data interface for communicating data to a data memory, which, inherently, stores the data.

Regarding claim 5, the memory break controller, discussed in reference to claim 1, comprises:

- A memory break control register, (see "control register", par. 0039, and 0047; see also par. 0040 and 0042 in which said control register receives a signal that places the debug circuitry in a JTAG debug mode), being activated by the break point address and a control signal inputted from the debugger controller, (note, again, par. 0042 in which the debug circuitry is armed and

set to allow breakpoint operations, which necessitates activating the register with a break point address);

- An address register, (see fig. 5, element 94), for storing the break point address inputted from the memory break control register, (note, also par. 0052);
- An address comparator for comparing the address of the data memory which is currently used by the processor core and the break point address stored in the address register, (see par. 0052);
- A data register for storing break point data associated with the break point address stored in the address register, (see fig. 5, element 110, and note par. 0053);
- A data comparator for comparing the data of the current address outputted from the data memory and the data of the break point address stored in the data register, (see par. 0053).

Regarding claim 6, Waldie teaches that the memory break control register comprises:

- A memory break enable flag for activating the memory break controller, (Fig. 6, bit 0);
- A data check flag, ("detector found bit"), being enabled when the content of the data of an address of the data memory which is identical to the break

point address stored in the address register is outputted, (see Fig. 6, bit 17; also see par. 0062);

- An address trace check flag, ("detector found bit"), also is enabled when the content of the address of the data memory which is identical to the break point address stored in the address register is outputted, (again, see Fig. 6, bit 17; and par. 0062).

As has been shown, the contents of the data register and address register storing data related to an address of the data memory which is identical to the break point address, are available to the host computer at all times, (see par. 0075). Therefore, it has been shown that said contents are outputted upon detecting that said addresses are identical.

Regarding claim 8, Waldie teaches a debugging apparatus for informing a data transition state, comprising:

- A debugger controller for outputting a control signal for performing a debugging, a memory break point address, and a break enable signal, (see par. 0029 in which the debug system is controlled by a debug controller; see also, par. 0042 in which the debug system is configured with a debug mode signal and is armed and set to allow breakpoint operations);

- A processor core being activated by said control signal, (par. 0030, lines 14-21), and reading data stored in a data memory or writing data, (see par. 0032);
- A memory break control register, (see "control register", par. 0039, and 0047; see also par. 0040 and 0042 in which said control register receives a signal that places the debug circuitry in a JTAG debug mode), being activated by the break point address and the control signal inputted from the debugger controller, (note, again, par. 0042 in which the debug circuitry is armed and set to allow breakpoint operations, which necessitates activating the register with a break point address);
- An address register, (see fig. 5, element 94), for storing the break point address inputted from the memory break control register, (note, also par. 0052);
- An address comparator for comparing the address of the data memory which is currently used by the processor and the break point address stored in the address register, (see par. 0052);
- A data register for storing break point data associated with the break point address stored in the address register, (see fig. 5, element 110, and note par. 0053);
- A data comparator for comparing the data of the current address outputted from the data memory and the data of the break point address stored in the data register, (see par. 0053).

Regarding claim 9, Waldie teaches a debugging method comprising the steps of:

- Outputting a break point address of a data memory to be observed and a break enable signal, when a processor is switched to a debugging mode, (see par. 0040 and 0042, in which breaking is enabled when control register R0 receives a configuration signal for debugging mode 1; also, note that the debug circuitry is armed and set to allow breakpoint operations, and note par. 0052 in which this necessitates outputting a break point address of a data memory);
- Storing the outputted break point address, (note par. 0052, in which the break point address is stored in register 94), and operating the processor in a general operation state, (see par. 0050);
- Comparing the stored break point address and the address of the data memory currently used by the processor, while the processor is being operated, (note, again, par. 0052);
- Outputting a break signal to suspend the processor, if the address of the data memory currently used by the processor and the stored break point address are identical to each other, (see, again, par. 0050, note lines 9-11); and
- Suspending the processor by the outputted break signal, and switching the processor to a debugging mode to debug the program, (note lines 9-11 of par. 0050, and see par. 0012 and lines 20-26 of par. 0031).

Regarding claim 10, Waldie teaches a method, as described in reference to claim 9, wherein, in the step of operating a processor, a memory break enable flag of a memory break controller is enabled according to an outputted break enable signal, (note par. 0042 in which the debug circuitry is enabled by a signal that configures the system in mode 1), and a data check flag and an address check flag are disabled, (note par. 0062, in which the detector found bit is set to indicate that a match was found by the break point detector, and note Fig. 5, in which a break point is detected based on a data check and an address check), in order to initialize the processor, (it is inherent that the processor be initialized with said flags disabled, in order to allow the flags to be enabled when a break point is detected), and then the break point address is stored, (note, again, par. 0042, in which debug circuitry is armed and set to allow breakpoint operations).

Regarding claim 11, Waldie teaches a method, as described in reference to claim 9, wherein the step of outputting a break signal comprises:

- A step in which when an address of the data memory currently used by the processor core and the stored break point address are identical to each other, it is determined whether the processor reads the data stored in the corresponding address or writes data, (see par. 0057, lines 31-34); and
- A step in which, in case of reading data, the address trace check flag and the data check flag of the memory break control register are enabled, (see par.

0062, in which the detector found bit, operating as an address trace check flag and a data check flag, is enabled when a match is found);

(see also rejection of claim 11 under the first paragraph of 35 U.S.C. 112)

Regarding claim 12, Waldie teaches a method, as described in reference to claim 11, wherein the step of comparing addresses comprises:

- A step in which, if the corresponding address of the data memory and the break point address are identical to each other, it is determined whether the processor read data stored in the data memory of the corresponding address or writes data in the data memory of the corresponding address, (see par. 0057, lines 31-34); and
- A step in which, in case of writing data, the data check flag of the memory break controller is enabled and a break signal for suspending the processor core is outputted, (see par. 0062, in which a data check flag is enabled; see 0050 in which the processor is suspended when a break point is detected).

Regarding claim 14, Waldie teaches a method, as described in reference to claim 11, wherein, if the processor core writes the data, (note par. 0057, lines 31-34), the data check flag of the memory break controller is set and the operation of the processor core is discontinued, (see par. 0062, in which a data check flag is enabled; see 0050 in which the processor is halted when a break point is detected).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3, 4, 7, 13, 15, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waldie et al, as applied to claims 1, 5, 6, 9, 11 and 12 above, and further in view of Torrey et al, (U.S. 6,145,123).

Regarding claim 3, Waldie teaches that the memory break controller transmits an address and data recognized as a break point, (note, again, par. 0052 and 0053, and see par. 0075, lines 26-34, in which the host may receive the information in the storage registers in the event of a breakpoint being detected), and activates an operation of the processor core, (note par. 0050).

Waldie fails to teach, explicitly, that the memory break controller outputs the used address and the data of the data memory to the host computer through the debugger controller until a break signal is outputted again. However, it does teach that the host computer may examine the results in the debug system storage registers in the background during a debugging event, (see par. 0075), and that the debugging process has a predetermined stopping point, (see par.0033).

Torrey teaches an apparatus in which, after a breakpoint has been detected, trace information is sent from a processor, through a debugger controller, (see fig. 1), to a host computer, (note, also, col. 6, lines 18-20, and col. 6, lines 66-67 to col. 7, lines 1-8). The trace data comprises all information necessary for allowing the host computer to monitor the debugging process. Torrey also teaches that the transmission of trace information should stop when a second breakpoint is detected, (see col. 4, lines 28-40).

Torrey and Waldie are analogous art because they are from the same field of endeavor, viz., debugging systems utilizing breakpoint instruction logic.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the transmission of trace information, as disclosed in Torrey, to the debugging system of Waldie, in order to provide a controllable means of determining a starting and stopping point of debug information being sent to a host computer.

One of ordinary skill in the art at the time of applicant's invention would have been motivated to combine the teachings because the trace information transmission teaching of Torrey offers a distinct advantage over the debug information monitoring capability of Waldie. Waldie teaches that debug information can be monitored by

the host computer after a breakpoint has been recognized. However, Waldie does not teach a controllable means of determining when said information should stop being monitored. Determining a starting and stopping point for monitoring debug information enables the host computer to store debug data related specifically to the debugging operation, which improves the host computer's ability to analyze said information to identify and correct any problems, (note Torrey, col. 3, lines 40-56). One of ordinary skill in the art, therefore, would have considered it obvious to combine the trace information transmission teaching of Torrey with the debugging system of Waldie, in order to improve the latter's ability to analyze debugging data monitored by the host computer.

As per claim 4, Waldie teaches that the host computer may examine the results in the debug system storage registers, (see par. 0075), and that the debug system is capable of recognizing when data or an address input into a register changes in comparison with the stored break point data or break point address, (see par. 0052 and 0053), in which case, the match data in the detector valid register is altered. Therefore, Waldie teaches that the host computer may recognize a data flow and change of the address and the data outputted from the memory break controller

Regarding claim 7, Waldie fails to teach, explicitly, that the memory break controller outputs the used address and the data of the data memory to the host computer through the debugger controller until a break signal is outputted again. However, it does teach that the host computer may examine the results in the debug system storage registers in the background during a debugging event, (see par. 0075), which entails that all addresses and data of the memory which is read from or written to by the processor are output to the host computer. Waldie also shows that the debugging process has a predetermined stopping point, (see par.0033).

Torrey teaches an apparatus in which, after a breakpoint has been detected, trace information is sent from a processor, through a debugger controller, (see fig. 1), to a host computer, (note, also, col. 6, lines 18-20, and col. 6, lines 66-67 to col. 7, lines 1-8). The trace data comprises all information necessary for allowing the host computer to monitor the debugging process. Torrey also teaches that the transmission of trace information should stop when a second breakpoint is detected, (or, when the content of the break address is updated; see col. 4, lines 28-40).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the transmission of trace information, as disclosed in Torrey, to the debugging system of Waldie, in order to provide a controllable means of determining a starting and stopping point of debug information being sent to a host computer.

One of ordinary skill in the art at the time of applicant's invention would have been motivated to combine the teachings because the trace information transmission teaching of Torrey offers a distinct advantage over the debug information monitoring capability of Waldie. Waldie teaches that debug information can be monitored by the host computer after a breakpoint has been recognized. However, Waldie does not teach a controllable means of determining when said information should stop being monitored. Determining a starting and stopping point for monitoring debug information enables the host computer to store debug data related specifically to the debugging operation, which improves the host computer's ability to analyze said information to identify and correct any problems, (note Torrey, col. 3, lines 40-56). One of ordinary skill in the art, therefore, would have considered it obvious to combine the trace information transmission teaching of Torrey with the debugging system of Waldie, in order to improve the latter's ability to analyze debugging data monitored by the host computer.

Regarding claim 15, Waldie teaches that, in the step of outputting a break signal, when the operation of the processor core is suspended by the break signal, the address and data of the corresponding data memory are transmitted, (see par. 0075 in which the host computer may examine the results in the debug system storage registers, which contain the address and data of the corresponding data memory).

Waldie fails to teach, explicitly, that the operation of the processor is activated to output an address and data of the data memory used by the processor until a break signal is outputted again. However, it does teach that the host computer may examine the results in the debug system storage registers in the background during a debugging event, (see par. 0075), and that the debugging process has a predetermined stopping point, (see par.0033).

Torrey teaches an apparatus in which, after a breakpoint has been detected, trace information is sent from a processor, through a debugger controller, (see fig. 1), to a host computer, (note, also, col. 6, lines 18-20, and col. 6, lines 66-67 to col. 7, lines 1-8). The trace data comprises all information necessary for allowing the host computer to monitor the debugging process. Torrey also teaches that the transmission of trace information should stop when a second breakpoint is detected, (see col. 4, lines 28-40).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the transmission of trace information, as disclosed in Torrey, to the debugging system of Waldie, in order to provide a controllable means of determining a starting and stopping point of debug information being sent to a host computer.

One of ordinary skill in the art at the time of applicant's invention would have been motivated to combine the teachings because the trace information transmission teaching of Torrey offers a distinct advantage over the debug information monitoring capability of Waldie. Waldie teaches that debug information can be monitored by the host computer after a breakpoint has been recognized. However, Waldie does not teach a controllable means of determining when said information should stop being monitored. Determining a starting and stopping point for monitoring debug information enables the host computer to store debug data related specifically to the debugging operation, which improves the host computer's ability to analyze said information to identify and correct any problems, (note Torrey, col. 3, lines 40-56). One of ordinary skill in the art, therefore, would have considered it obvious to combine the trace information transmission teaching of Torrey with the debugging system of Waldie, in order to improve the latter's ability to analyze debugging data monitored by the host computer.

Regarding claim 13, Waldie fails to teach that, in the method described in reference to claim 12 above, if it is determined that the processor reads the data, the next address of the data memory to be used by the processor core and the break point address are compared. However, Waldie does teach that the host computer may examine the results in the debug system storage registers in the background during

a debugging event, (see par. 0075), and that the system is capable of detecting a break point on a memory read operation, (see par. 0057, lines 31-34).

Torrey teaches an apparatus in which, after a breakpoint has been detected, trace information is sent from a processor, through a debugger controller, (see fig. 1), to a host computer, (note, also, col. 6, lines 18-20, and col. 6, lines 66-67 to col. 7, lines 1-8). The trace data comprises all information necessary for allowing the host computer to monitor the debugging process. Torrey also teaches that the transmission of trace information should stop when a second breakpoint is detected, (see col. 4, lines 28-40). Therefore, Torrey teaches that, after a breakpoint is detected, the next address of the memory to be used by the processor core and the break point address are compared.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the transmission of trace information, as disclosed in Torrey, to the debugging system of Waldie, in order to provide a controllable means of determining a starting and stopping point of debug information being sent to a host computer. Moreover, one of ordinary skill in the art would consequently find it obvious to combine the step of comparing the next address of the data memory with the break point address with the teachings of Waldie, to enable said stopping point determination.

One of ordinary skill in the art at the time of applicant's invention would have been motivated to combine the teachings because the trace information transmission teaching of Torrey offers a distinct advantage over the debug information monitoring capability of Waldie. Waldie teaches that debug information can be monitored by the host computer after a breakpoint has been recognized. However, Waldie does not teach a controllable means of determining when said information should stop being monitored. Determining a starting and stopping point for monitoring debug information enables the host computer to store debug data related specifically to the debugging operation, which improves the host computer's ability to analyze said information to identify and correct any problems, (note Torrey, col. 3, lines 40-56). One of ordinary skill in the art, therefore, would have considered it obvious to combine the trace information transmission teaching of Torrey with the debugging system of Waldie, in order to improve the latter's ability to analyze debugging data monitored by the host computer. Moreover, one of ordinary skill in the art would be, consequently, motivated to combine the step of comparing the next address of the data memory with the break point address with the teachings of Waldie, to enable the trace information transmission teaching of Torrey.

Regarding claim 16, Waldie teaches a debugging method for informing a data transition state, comprising:

- A step in which when a processor is switched into a debugging mode, a break point address of a data memory to be observed, and a break enable signal are outputted, (see par. 0040 and 0042, in which breaking is enabled when control register R0 receives a configuration signal for debugging mode 1; also, note that the debug circuitry is armed and set to allow breakpoint operations, and note par. 0052 in which this necessitates outputting a break point address of a data memory);
- A step in which the outputted break point address is stored, (note par. 0052, in which the break point address is stored in register 94);
- A step in which the stored break point address and an address of a data memory currently used by a processor core are compared, (see par. 0052);
- A step in which, when the address of the data memory currently used by the processor core and the stored break point address are identical to each other, it is determined whether the processor core reads data stored in the corresponding address or writes data, (see par. 0057, lines 31-34);
- A step in which, if it is determined that the processor core writes data in a corresponding address, (note, again, par. 0057, lines 31-34), a data check flag of a memory break controller is enabled and a break signal for suspending the processor core is outputted, (see par. 0062, in which a data check flag is enabled; see 0050 in which the processor is suspended when a break point is detected);

- A step in which, when the processor core is suspended by the outputted break signal, the address and the data of the corresponding data memory are outputted, (see par. 0075, lines 26-34, in which the address and data of the corresponding data memory, which are stored in the debug system registers, are available to the host system upon a break point event); and
- A step in which the operation of the processor core is then activated, (see par. 0050, lines 16-17)

Waldie fails to teach, explicitly, that the operation of the processor is activated to output an address and data of the data memory used by the processor until a break signal is outputted again. However, it does teach that the host computer may examine the results in the debug system storage registers in the background during a debugging event, (see par. 0075), and that the debugging process has a predetermined stopping point, (see par.0033).

Torrey teaches an apparatus in which, after a breakpoint has been detected, trace information is sent from a processor, through a debugger controller, (see fig. 1), to a host computer, (note, also, col. 6, lines 18-20, and col. 6, lines 66-67 to col. 7, lines 1-8). The trace data comprises all information necessary for allowing the host computer to monitor the debugging process. Torrey also teaches that the transmission of trace information should stop when a second breakpoint is detected, (see col. 4, lines 28-40).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the transmission of trace information, as disclosed in Torrey, to the debugging system of Waldie, in order to provide a controllable means of determining a starting and stopping point of debug information being sent to a host computer.

One of ordinary skill in the art at the time of applicant's invention would have been motivated to combine the teachings because the trace information transmission teaching of Torrey offers a distinct advantage over the debug information monitoring capability of Waldie. Waldie teaches that debug information can be monitored by the host computer after a breakpoint has been recognized. However, Waldie does not teach a controllable means of determining when said information should stop being monitored. Determining a starting and stopping point for monitoring debug information enables the host computer to store debug data related specifically to the debugging operation, which improves the host computer's ability to analyze said information to identify and correct any problems, (note Torrey, col. 3, lines 40-56). One of ordinary skill in the art, therefore, would have considered it obvious to combine the trace information transmission teaching of Torrey with the debugging system of Waldie, in order to improve the latter's ability to analyze debugging data monitored by the host computer.

Regarding claim 17, and as applied to claim 16, Waldie teaches that the system is capable of detecting a break point on a data memory read operation, (see par. 0057, lines 31-34). Torrey teaches that the next address of the memory used by the processor core and the break point address are compared, upon detecting a first break point, (this step is inherent to detecting a second break point in order to stop trace information transmission, see col. 3, lines 28-40).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cheung et al, (US 2002/0188813 A1) teaches a hardware breakpoint generator capable of producing a breakpoint request on a memory read or write access in a data memory or program memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (703) 605-1211. After approximately October 15, 2004 the examiner's telephone number will

change to (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Aaron D Matthew
Examiner
Art Unit 2114

ADM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100